IN THE CLAIMS:

2. (PREVIOUSLY PRESENTED) A LOC type semiconductor package according to claim 8, wherein:

the outer portions of the general leads extend from the molding resin; and

the outer portions of the stable leads extend from the molding resin.

4. (PREVIOUSLY PRESENTED) A LOC type semiconductor package according to claim 13, wherein:

the attachment section of the stable leads includes a substantially greater width than an adjacent inner portion of the stable leads.

8. (PREVIOUSLY PRESENTED) A LOC type semiconductor package, comprising:

a semiconductor chip having a chip periphery and a plurality of bonding pads, the bonding pads being arranged within the chip periphery;

a plurality of general leads, the general leads having inner and outer portions, the inner portions being spaced from and not crossing the chip periphery;

a first plurality of wires extending between corresponding bond pads and inner portions of the general leads, thereby extending across the chip periphery;

as many as four stable leads, the stable leads having inner and outer portions, the inner portions extending over the chip periphery and arranged in a generally planar relationship with the inner portions of the general leads;

an adhesive composition arranged between the semiconductor chip and an attachment section of the inner portion of each stable lead;

a second plurality of wires within the chip periphery extending between corresponding bond pads and inner portions of the stable leads; and

a molding resin encapsulating the semiconductor chip, the inner portions of the general leads, the inner portions of the stable leads, the adhesive composition, the first plurality of wires and the second plurality of wires.

9. (PREVIOUSLY PRESENTED) A LOC type semiconductor package according to claim 8, wherein:

the plurality of bonding pads are arranged in a single row.

10. (PREVIOUSLY PRESENTED) A LOC type semiconductor package according to claim 9, wherein:

the single row is arranged in a generally longitudinal direction and generally centered on the semiconductor chip.

11. (PREVIOUSLY PRESENTED) A LOC type semiconductor package according to claim 8, wherein:

the plurality of bonding pads are arranged in two parallel rows.

12. (PREVIOUSLY PRESENTED) A LOC type semiconductor package according to claim 11, wherein:

the parallel rows are arranged in a generally longitudinal direction about a central longitudinal axis of the semiconductor chip.

13. (PREVIOUSLY PRESENTED) A LOC type semiconductor package according to claim 8, wherein:

the attachment sections of the stable leads are configured to increase the bond strength between the attachment section and the adhesive composition.

14. (PREVIOUSLY PRESENTED) A LOC type semiconductor package according to claim 13, wherein:

the attachment sections of the stable leads have a serpentine configuration.

15. (PREVIOUSLY PRESENTED) A LOC type semiconductor package according to claim 13, wherein:

the attachment sections of the stable leads are configured to form an open structure having an inside edge and an outside edge.

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IN THE DRAWINGS:

The attached sheet of drawing presents a new FIG. 8, which generally corresponds to original FIG. 3, but reflects a conventional double-row bond pad configuration to illustrate an embodiment of the LOC type semiconductor package as recited in claims 11 and 12.

Attachment: New Drawing Sheet